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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,074	07/25/2003	Michel A. Moacanin	FULCP010	3500

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,074	MOACANIN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7-10,16-32,37 and 43-48* is/are rejected.

7)☒ Claim(s) *3-6,11-15,33-36 and 38-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-48 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 9/24/03 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Allowable Subject Matter

Claims 3-6, 11-15, 33-36, and 38-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7-10, 16-22, 24, 31, 32, 37, and 43-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Reis et al. U.S. Patent No. 6,807,644.

As per claim 1, Reis et al. teach the claimed test interface for providing test access by synchronous test equipment to an asynchronous circuit, the test interface comprising (column 3 lines 44-51): synchronous-to-asynchronous (S2A) conversion circuitry (transceiver figure 2 TR1) operable to receive synchronous input data serially from the synchronous test equipment and convert the synchronous input data to asynchronous input data; asynchronous (Figure 2 ATP) logic operable to transmit the asynchronous input data to a first test register in the asynchronous circuit, and to transmit asynchronous output data received from a second test register in the asynchronous circuit, the asynchronous output data resulting from application of the asynchronous input data to the asynchronous circuit (Abstract), operation of the asynchronous logic being synchronized at least in part with a clock signal associated with the synchronous test equipment (column 4 lines 52-64); and asynchronous-to-synchronous (A2S) conversion (figure 2 TR2) circuitry operable to receive the asynchronous output data from the asynchronous logic, convert the asynchronous output data to synchronous output data, and serially transmit the synchronous output data to the synchronous test equipment (Abstract, column 3 line 52 through column 4 line 5).

As per claim 2, Reis et al teach the asynchronous logic comprises a shift register, which is operable alternately to receive the asynchronous input data serially from the S2A conversion circuitry and transmit the asynchronous output data serially to the A2S conversion circuitry (column 3 lines 16-27).

As per claim 7, Reis et al teach an interface controller operable to control operation of the asynchronous logic in accordance with the clock signal (column 4 lines 52-66).

As per claim 8, Reis et al. teach the interface controller comprises a finite state machine having a plurality of associated states (column 4 lines 52-66).

As per claim 9, Reis et al. teach selected ones of the plurality of states correspond to operations of the shift register, the shift register operations including a shift operation for shifting in the asynchronous input data and shifting out the asynchronous output data, an update operation for transmitting the asynchronous input data to the first test register, and a capture operation for receiving the asynchronous output data from the second test register (column 4 lines 52-66).

As per claim 10, Reis et al. teach the shift register is operable to perform a plurality of operations including a shift operation for shifting in the asynchronous input data and shifting out the asynchronous output data, an update operation for transmitting the asynchronous input data to the first test register, and a capture operation for receiving the asynchronous output data from the second test register (column 4 lines 52-66).

As per claims 16 and 17, Reis et al. teach the asynchronous logic is operable to transmit the asynchronous input and output data in accordance with a multi-phase handshake protocol (column 4 lines 6-14).

As per claims 18, and 19, Reis et al. teach the test interface is part of a JTAG compliant interface (Abstract).

As per claim 20, Reis et al. teach the JTAG compliant interface further comprises at least one synchronous register for providing test access to a synchronous circuit associated with the asynchronous circuit (column 3 lines 16-21).

As per claim 21, Reis et al. teach the at least one synchronous register comprises any of a bypass register, a device identification register, and a boundary scan register (column 3 lines 21-33).

As per claim 22, Reis et al. teach to the use of an integrated circuit with this interface (column 1 lines 8-15)

As per claim 24, Reis et al. teach the integrated circuit comprises at least one of a programmable logic device, a field-programmable gate array, an application-specific integrated circuit, a microprocessor, and a system on a chip (column 6 lines 10-20).

As per claim 31, Reis et al. teach the claimed method for testing an asynchronous circuit using synchronous test equipment (column 3 lines 44-51), comprising: converting synchronous input data (transceiver figure 2 TR1) received from the synchronous test equipment to asynchronous input data; transmitting the asynchronous input data to a first test register in the asynchronous circuit (Figure 2 ATP); receiving asynchronous output data from a second test register in the asynchronous circuit (Abstract), the asynchronous output data resulting from application of the asynchronous input data to the asynchronous circuit (column 4 lines 52-64); and converting the asynchronous output data to synchronous output data; and serially transmitting the synchronous output data to the synchronous test equipment (figure 2

TR2); wherein transmission and reception of the asynchronous input and output data are synchronized at least in part with a clock signal associated with the synchronous test equipment (Abstract, column 3 line 52 through column 4 line 5).

As per claim 32, Reis et al. teach transmitting the asynchronous input data to the first test register comprises receiving the asynchronous input data with a shift register, and wherein receiving the asynchronous output data from a second test register comprises receiving the asynchronous output data with the shift register (column 3 lines 16-27).

As per claim 37, Reis et al. teach receiving the asynchronous input data with the shift register comprises shifting in the asynchronous input data and shifting out previous asynchronous output data (column 3 lines 16-27). The examiner would also like to point out that it is inherent in a shift register that when something is shifted in whatever was in the register is shifted out.

As per claims 43 and 44, Reis et al. teach transmitting of the asynchronous input and receiving of the asynchronous output data is done in accordance with a multi-phase handshake protocol. (Column 4 lines 6-14)

As per claims 45 and 46, Reis et al. teach testing of the asynchronous circuit using the synchronous test equipment is done in accordance with a JTAG protocol. (Abstract)

As per claim 47, Reis et al. teach providing at least one synchronous register for facilitating test access to a synchronous circuit associated with the asynchronous circuit (column 3 lines 16-21).

As per claim 48, Reis et al. teach the at least one synchronous register comprises any of a bypass register, a device identification register, and a boundary scan register (column 3 lines 16-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reis et al. U.S. Patent No. 6,807,644 in view of Banerjee et al. U.S. Patent No. 5,958,077.

As per claims 25-29, Reis et al. teach the claimed test interface for providing test access by synchronous test equipment to an asynchronous circuit, the test interface comprising (column 3 lines 44-51): synchronous-to-asynchronous (S2A) conversion circuitry (transceiver figure 2 TR1) operable to receive synchronous input data serially from the synchronous test equipment and convert the synchronous input data to asynchronous input data; asynchronous (Figure 2 ATP) logic operable to transmit the asynchronous input data to a first test register in the asynchronous circuit, and to transmit asynchronous output data received from a second test register in the asynchronous circuit, the asynchronous output data resulting from application of the asynchronous input data to the asynchronous circuit (Abstract), operation of the asynchronous logic being synchronized at least in part with a clock signal associated with the synchronous test equipment (column 4 lines 52-64); and asynchronous-to-synchronous (A2S) conversion (figure 2 TR2) circuitry operable to receive the asynchronous output data from the asynchronous logic, convert the asynchronous output data to synchronous output data, and serially transmit the synchronous output data to the synchronous test equipment (Abstract, column 3 line 52 through column 4

line 5). Not explicitly disclosed by Reis et al is the computer readable medium containing the following:

However, in an analogous art, Banerjee et al. teach a synchronous test model (STM) that accurately models an asynchronous circuit under test is used to impose a fundamental mode of operation during a test generation. By forcing the circuit to operate in the fundamental mode, a new input cannot be applied to the circuit until it has stabilized. In this inventive manner, test generation is constrained without modifying a synchronous test algorithm. Specifically, this operates by 1) Constructing an STM for the asynchronous circuit assuming a user-specified cycle length time or an estimated time; 2) Creating a target fault list which contains only faults in the asynchronous circuit; 3) Generating test patterns on the STM using a known, synchronous test generator; 4) Translating these test patterns into sequences for the asynchronous circuit; and 5) Validating the translated patterns by fault simulation on the asynchronous circuit. Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the system of Banerjee et al. within the system of Reis et al. As suggested by Reis et al. (column 7 lines 44-59).

Claims 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reis et al. U.S. Patent No. 6,807,644.

As per claims 23 and 30, the examiner would like to point out that it is well known in the art for the following structures to be used within the above claimed test environment see the cited references. The integrated circuit comprises any of a CMOS

integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit, and set of semiconductor processing masks representative of at least a portion of the test interface would have been obvious to a person having ordinary skill in the art at the time of this invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

IBM TDB: NN8607813 "Method to Synchronize an Asynchronous IBM Series/1 Interface to Allow Testing on a Synchronous Tester" IBM Technical Disclosure Bulletin, July 1986, US VOLUME:29, ISSUE:2 PAGE: 813 - 815 Publication Date: July 1, 1986 (19860701)

"Low-power synchronous-to-asynchronous- to-synchronous interlocked pipelined CMOS circuits operating at 3.3-4.5 GHz" by Schuster et al. This paper appears in: IEEE Journal of Solid-State Circuits Publication Date: Apr 2003 Volume: 38, Issue: 4
On page(s): 622- 630 ISSN: 0018-9200 INSPEC Accession Number: 7565233

This paper teaches an Interlocked pipelined CMOS (IPCMOS),having a new asynchronous set of clock circuits suitable for high-frequency and low-power operation. In IPCMOS, the reduced power results from enabling the local clocks only when there is an operation to perform and from a simple single-stage latch. The single-stage latch can be used because the locally generated clocks driving adjacent stages are not enabled simultaneously. The combination of enabling the clocks only when there is an operation

to perform and the simple latch can lower power by a factor of five to ten times in many applications. In IPCMOS, the staggered local clocks also result in a significant reduction of dynamic Ldi/dt noise. In addition to the locally generated interlocked clocks and the single-stage latch, unique circuits that combine the function of a static NOR and an input switch are key to achieving high performance and minimizing the overhead in the interlocking. IPCMOS also provides a way to implement the interface between asynchronous and synchronous portions of a design, thereby giving the approach a great deal of flexibility by making it possible to drop IPCMOS into portions of an existing synchronous design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt 1-20-07
Cynthia Britt
Primary Examiner
Art Unit 2138